

### CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

### IN THE CLAIMS

**Note:** No amendments are being made to the claims with this response. However, a complete listing of the claims is provided below for reference purposes.

1. (Previously Presented) A test configuration comprising:
  - an integrated circuit to be tested;
  - an I/O pad of the integrated circuit;
  - an output buffer, wherein an output terminal of the output buffer is coupled to the I/O pad;
  - a current injector on the integrated circuit coupled to the I/O pad for injecting a current at the I/O pad; and
  - a detector on the integrated circuit coupled to the I/O pad for detecting a logic level of the I/O pad.
2. (Canceled)
3. (Previously Presented) The test configuration of claim 1 wherein the output buffer is a tristate buffer.
4. (Original) The test configuration of claim 1 further comprising an input buffer, wherein an input terminal of the input buffer is coupled to the I/O pad.
5. (Original) The test configuration of claim 1 wherein the current injector is selectively enabled by a memory bit.

6. (Original) The test configuration of claim 1 wherein the current injector is a resistive element on the integrated circuit coupled between the I/O pad and a voltage reference node.
7. (Original) The test configuration of claim 6 wherein the resistive element is a transistor.
8. (Original) The test configuration of claim 7 wherein a gate of the transistor is coupled to a memory bit.
9. (Original) The test configuration of claim 6 wherein the voltage reference node is a power node.
10. (Original) The test configuration of claim 6 wherein the voltage reference node is a ground node.
11. (Original) The test configuration of claim 1 wherein the integrated circuit is one of a plurality of integrated circuits on a wafer.
12. (Original) The test configuration of claim 1 wherein the integrated circuit comprises a plurality of I/O pads, the test configuration further comprising:
  - a probe card coupled to a subset of the plurality of I/O pads; and
  - automated test equipment coupled to the probe card.
13. (Original) The test configuration of claim 1 wherein the integrated circuit is a programmable logic device.
14. (Original) The test configuration of claim 1 wherein the detector is a boundary scan cell.

15. (Previously Presented) A test configuration comprising:
- an integrated circuit to be tested;
  - an I/O pad of the integrated circuit;
  - a current injector on the integrated circuit coupled to the I/O pad for injecting a current at the I/O pad;
  - wherein the current injector is a first transistor coupled between the I/O pad and a power node;
  - a detector on the integrated circuit coupled to the I/O pad for detecting a logic level of the I/O pad
  - a second transistor coupled between the I/O pad and a ground node;
  - a first memory bit coupled to a gate of the first transistor; and
  - a second memory bit coupled to a gate of the second transistor.
16. (Original) The test configuration of claim 15 further comprising:
- a tristate output buffer having an output terminal coupled to the I/O pad;
- and
- an input buffer having an input terminal coupled to the I/O pad.
17. (Previously Presented) A method for testing an I/O pad of an integrated circuit, the method comprising:
- enabling a current injector on the integrated circuit coupled to the I/O pad;
  - driving an output value at the I/O pad through an output buffer coupled to the I/O pad;
  - enabling a detector on the integrated circuit coupled to the I/O pad; and
  - after enabling the detector, detecting a logic value of the I/O pad.

18. (Original) The method of claim 17 further comprising:  
    comparing the detected logic value with an expected value; and  
    if the detected logic value and the expected value do not match, rejecting  
the integrated circuit.
19. (Canceled)
20. (Original) The method of claim 17 wherein the output value is a logic low,  
further comprising:  
    if the detected logic value is not a logic low, rejecting the integrated  
circuit.
21. (Original) The method of claim 20 wherein the output value is a first output  
value and wherein the detected logic value is a first detected logic value, further  
comprising:  
    driving a second output value at the I/O pad through the output buffer,  
wherein the second output value is a logic high;  
    detecting a second logic value of the I/O pad; and  
    if the second detected logic value is not a logic high, rejecting the  
integrated circuit.
22. (Original) The method of claim 21 wherein the step of rejecting the integrated  
circuit comprises discarding the integrated circuit after the integrated circuit is diced  
from a wafer.

23. (Original) The method of claim 17 further comprising:  
receiving an input value through an input buffer coupled to the I/O pad.
24. (Original) The method of claim 17 further comprising:  
storing the detected logic value in a boundary scan cell of the integrated circuit;  
scanning out the stored logic value.
25. (Original) The method of claim 24 further comprising:  
receiving the scanned logic value through a probe card; and  
analyzing the received logic value with automated test equipment at wafer sort.
26. (Original) The method of claim 25 further comprising stepping the probe card over each of a plurality of integrated circuits on a wafer.